The list of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. A method for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising:

selecting first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad; and then

selecting second data from another of the plurality of memory regions for output from the memory device via the input/output pad.

2. The method of Claim 1, wherein selecting first and second data is preceded by reading data from the plurality of memory regions in the memory array.

3. The method of Claim 1, wherein the first and second data are both selected from memory regions sharing a row select control line or from memory regions sharing a column select control line.

4. The method of Claim 1, wherein one of the first and second data is selected from memory regions sharing a row select control line, and wherein the other of the first and second data is selected from memory regions sharing a column select control line.

5. The method of Claim 1, further comprising replacing a defective row select control line with a redundant row select control line from a row redundant memory cell array.

6. The method of Claim 1, further comprising replacing a defective column select control line with a redundant column select control line from a column redundant memory cell array.

7. The method of Claim 1, wherein the first data is selected in response to a first control signal, and wherein the second data is selected in response to a second control signal.

8. The method of Claim 1, wherein the memory device operates at a single data rate.

9. The method of Claim 1, wherein the memory device operates at a double data rate.

10. A method for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising:

writing test data to a plurality of memory regions in the memory array;

reading the test data from the plurality of memory regions;

comparing the test data from the plurality of memory regions to produce comparison data that corresponds to the plurality of memory regions;

selecting first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad; and then

selecting second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad.

11. A circuit for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising:

a selecting circuit configured to select first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad, and then select second data from another of the plurality of memory regions for output from the memory device via the input/output pad.

12. The circuit of Claim 11, further comprising a comparator circuit that is configured to read data from the plurality of memory regions and produce comparison data corresponding to the plurality of memory regions, wherein the selecting circuit selects the first and second data from the comparison data.

13. The circuit of Claim 11, wherein the selecting circuit selects both of the first and second data from memory regions sharing a row select control line or from memory regions sharing a column select control line.

14. The circuit of Claim 11, wherein the selecting circuit selects one of the first and second data from memory regions sharing a row select control line, and selects the other of the first and second data from memory regions sharing a column select control line.

15. The circuit of Claim 11, further comprising a row redundant memory cell array for replacing a defective row select control line with a redundant row select control line.

16. The circuit of Claim 11, further comprising a column redundant memory cell array for replacing a defective column select control line with a redundant column select control line.

17. The circuit of Claim 11, wherein the memory device operates at a single data rate.

18. The circuit of Claim 11, wherein the memory device operates at a double data rate.

19. The circuit of Claim 11, wherein the selecting circuit selects the first data in response to a first control signal, and selects the second data in response to a second control signal.

20. The circuit of Claim 11, wherein the circuit for testing the memory array is internal to the semiconductor memory device.

21. A circuit for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising:

a multiplexer configured to write test data to a plurality of memory regions in the memory array;

a comparator circuit configured to read the test data from the plurality of memory regions and produce comparison data that corresponds to the plurality of memory regions; and

a selecting circuit configured to select first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad, and then select second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad.

22-35 Canceled.